

FIG. 1
(*PRIOR ART*)

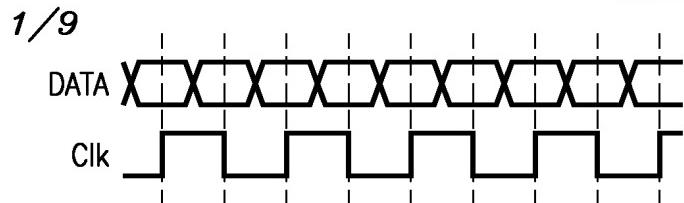


FIG. 2
(*PRIOR ART*)

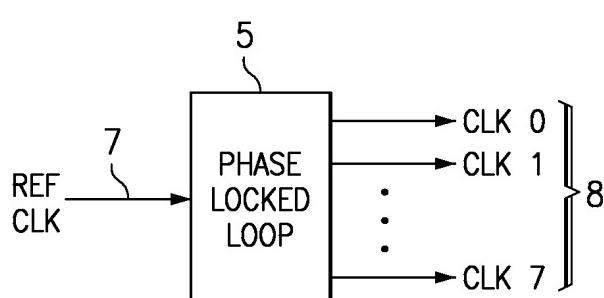


FIG. 3
(*PRIOR ART*)

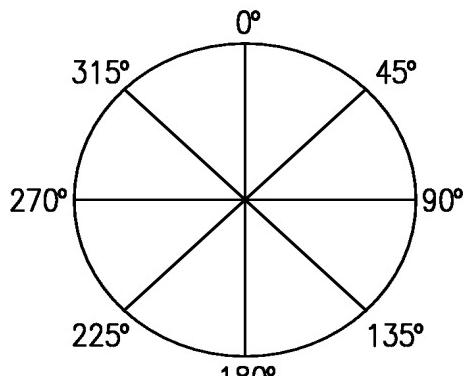


FIG. 4
(*PRIOR ART*)

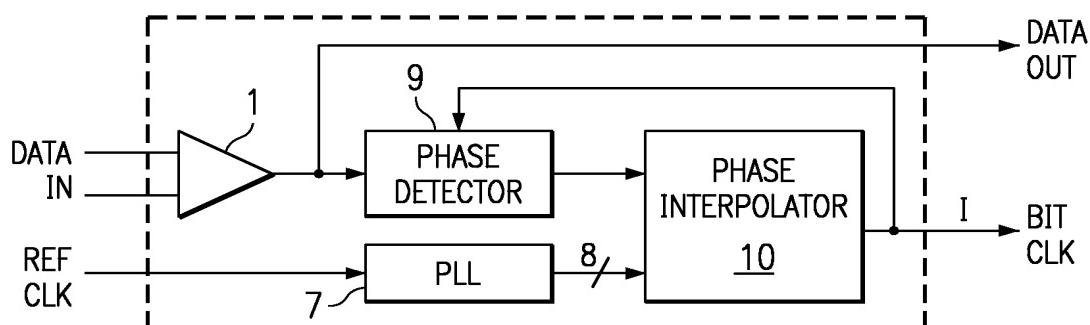


FIG. 5
(*PRIOR ART*)

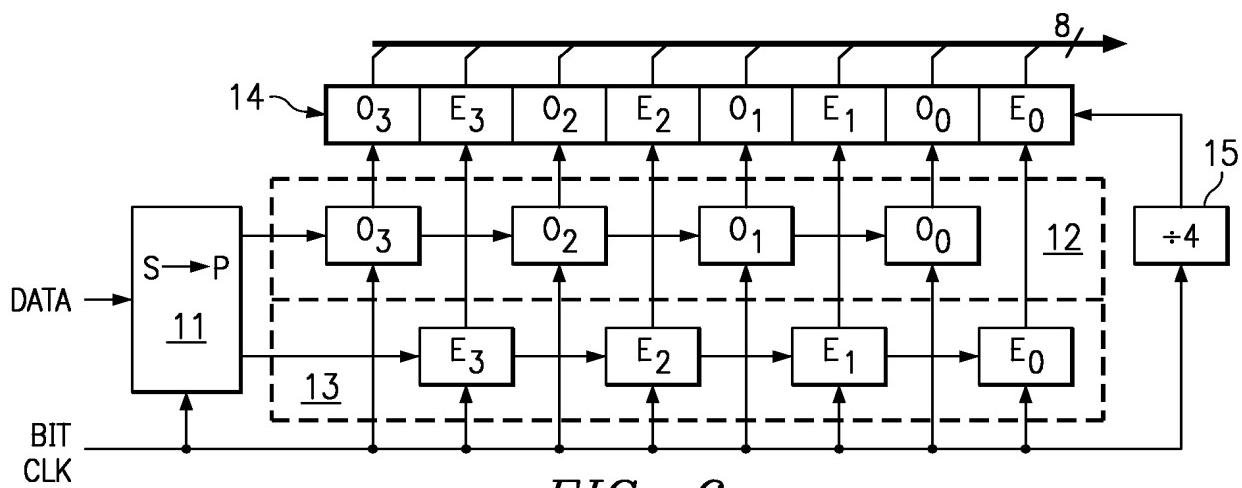


FIG. 6

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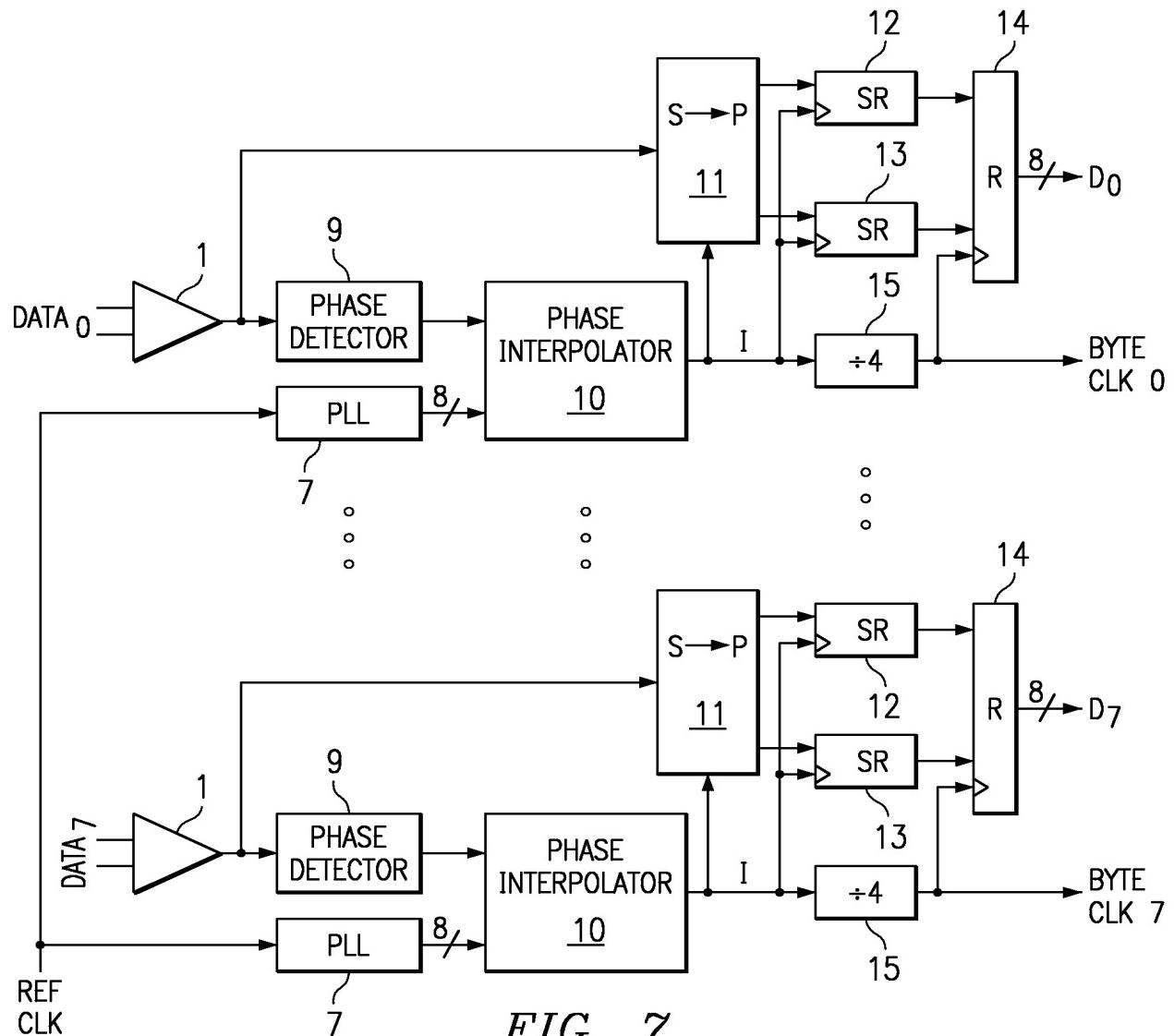


FIG. 7

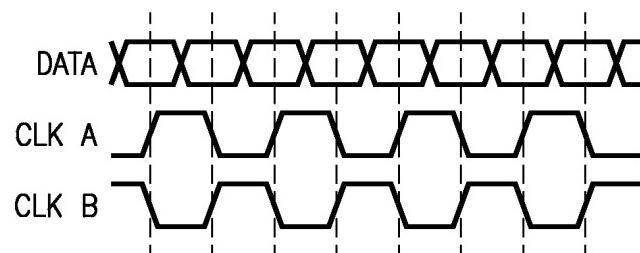


FIG. 8

FIG. 9

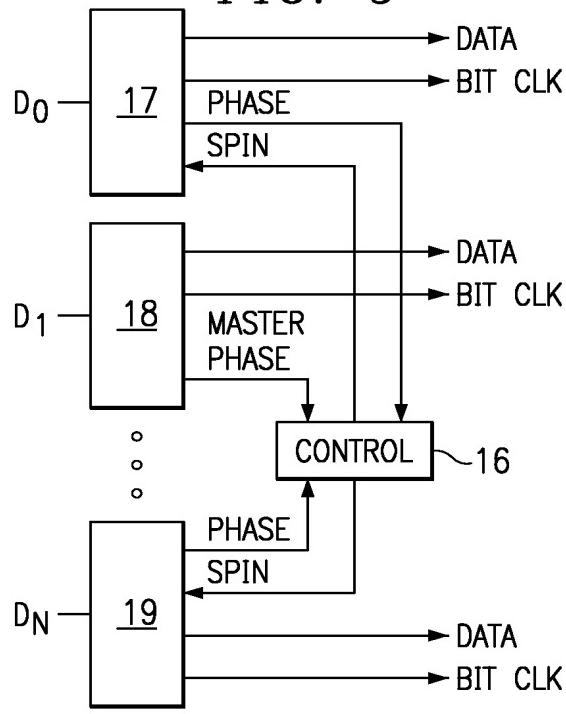


FIG. 10

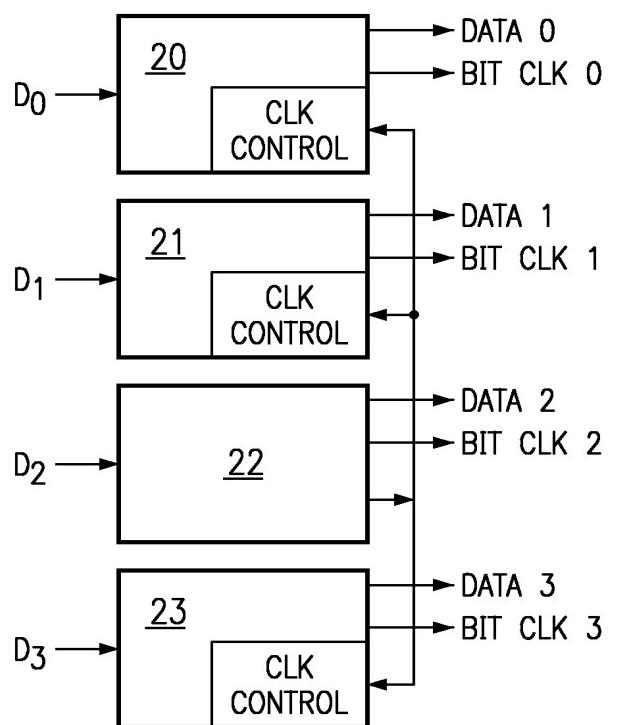
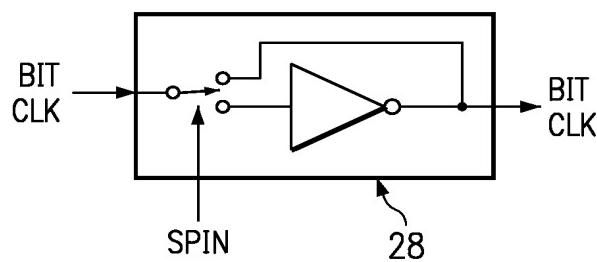


FIG. 9a



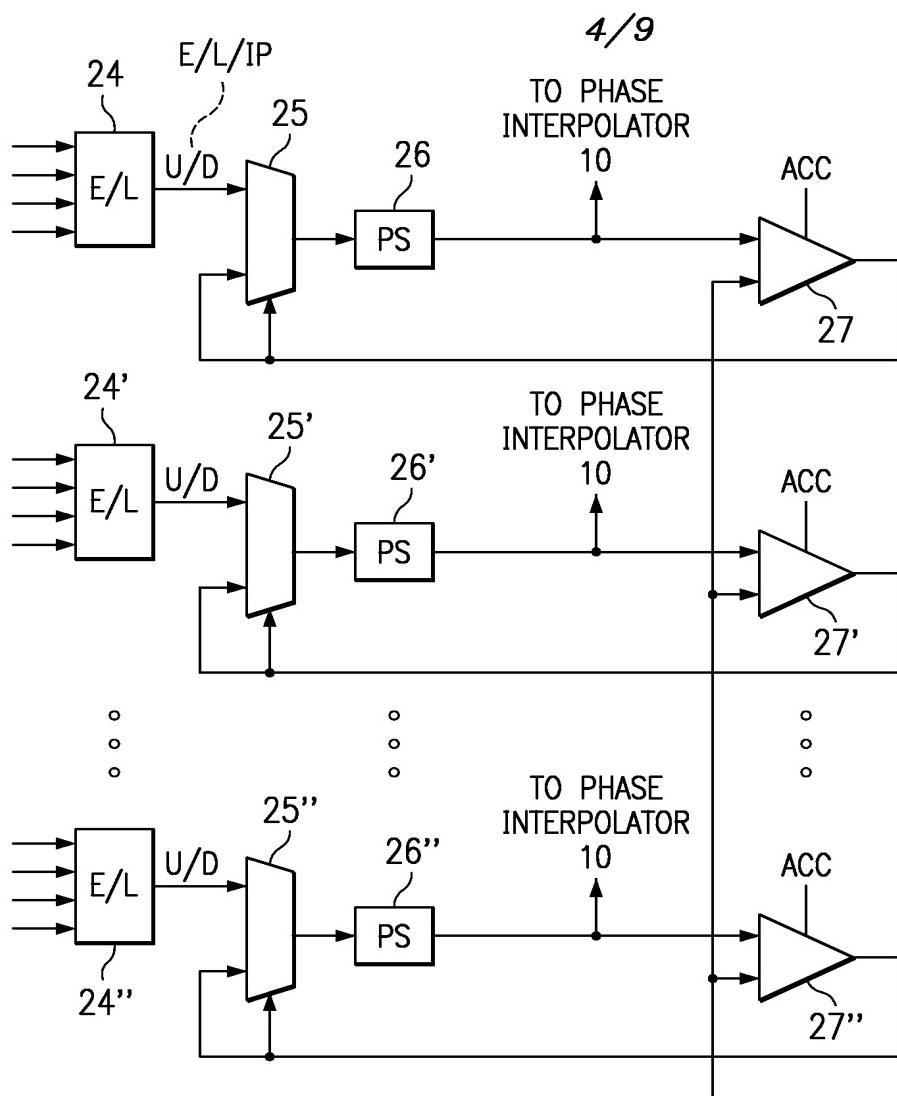


FIG. 11

MASTER BIT CLOCK
PHASE FROM 22

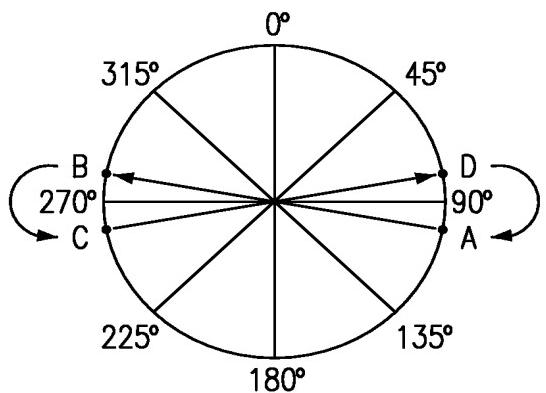


FIG. 12

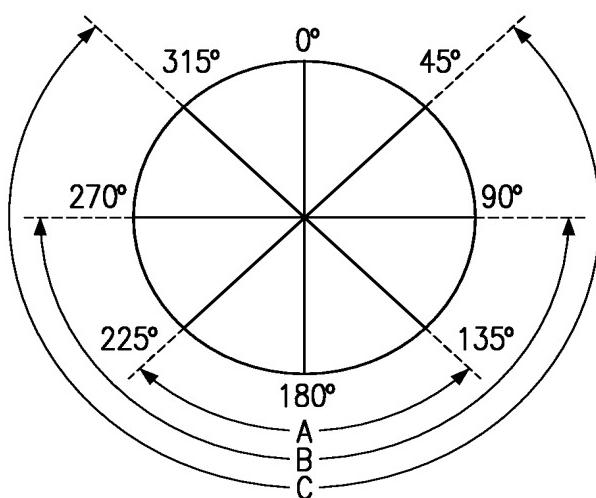


FIG. 13

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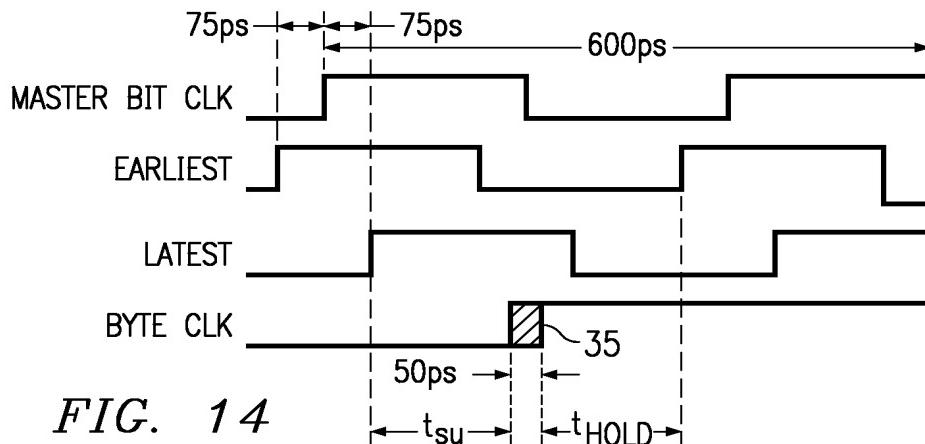


FIG. 14

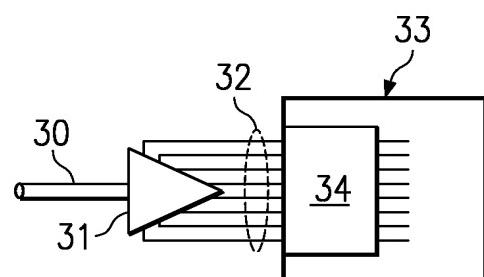


FIG. 15

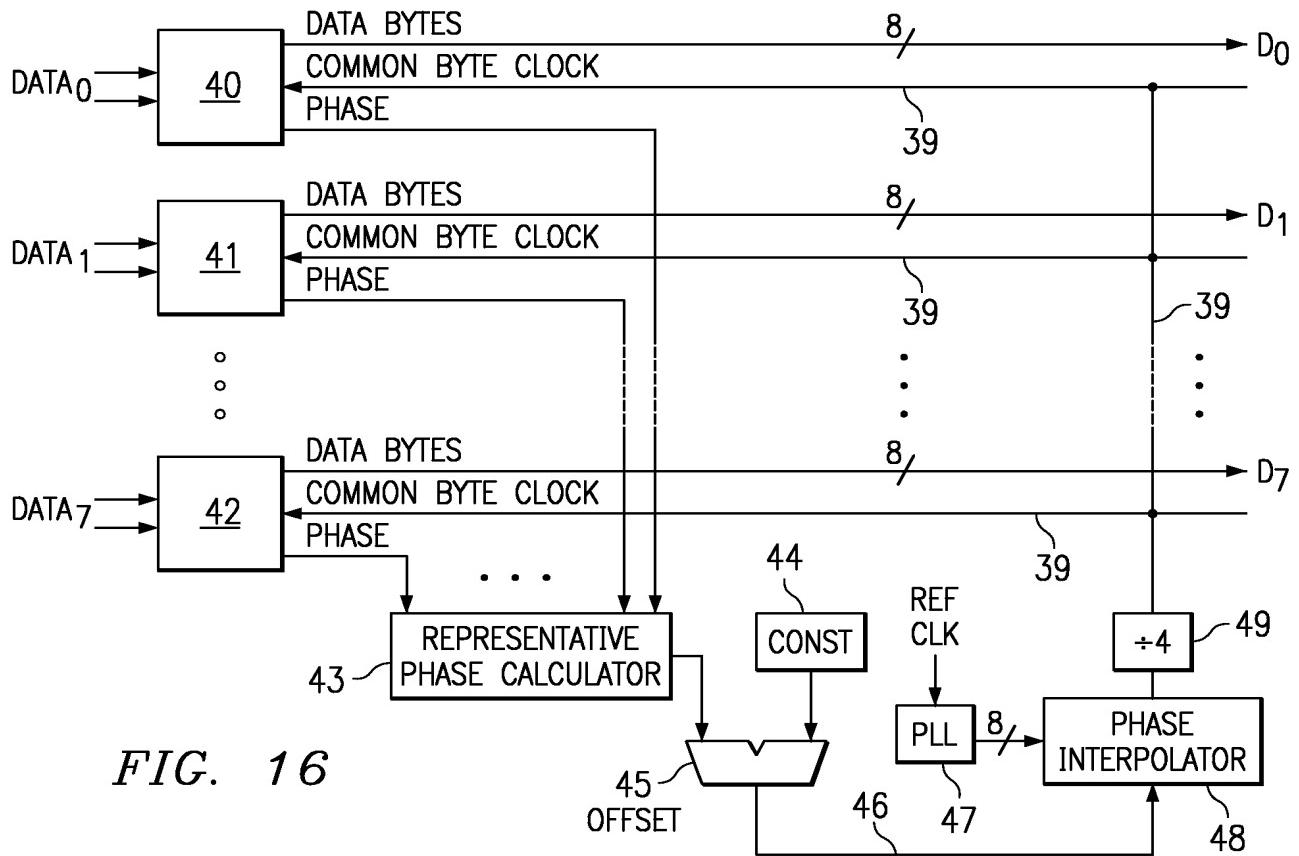


FIG. 16

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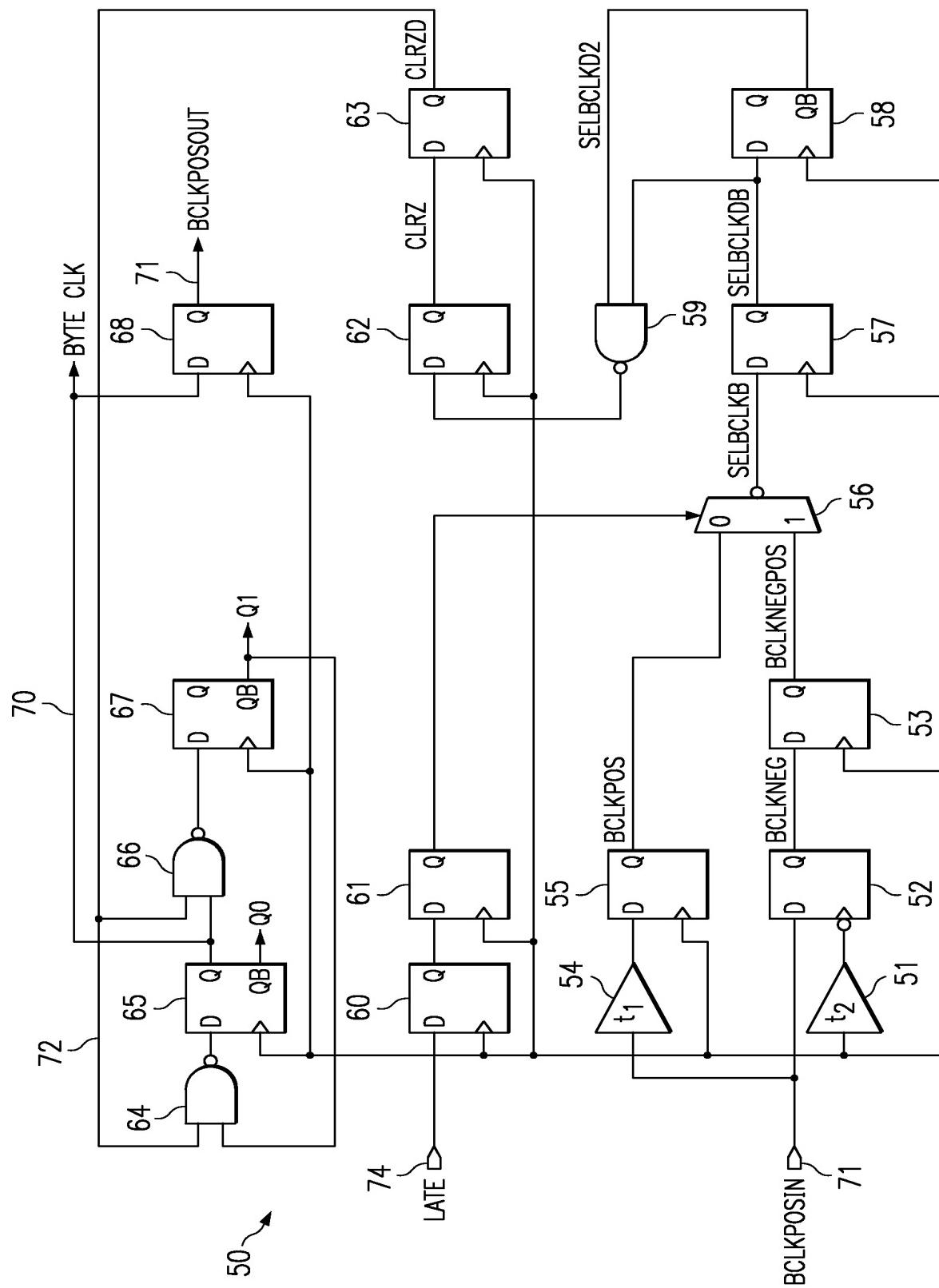


FIG. 17

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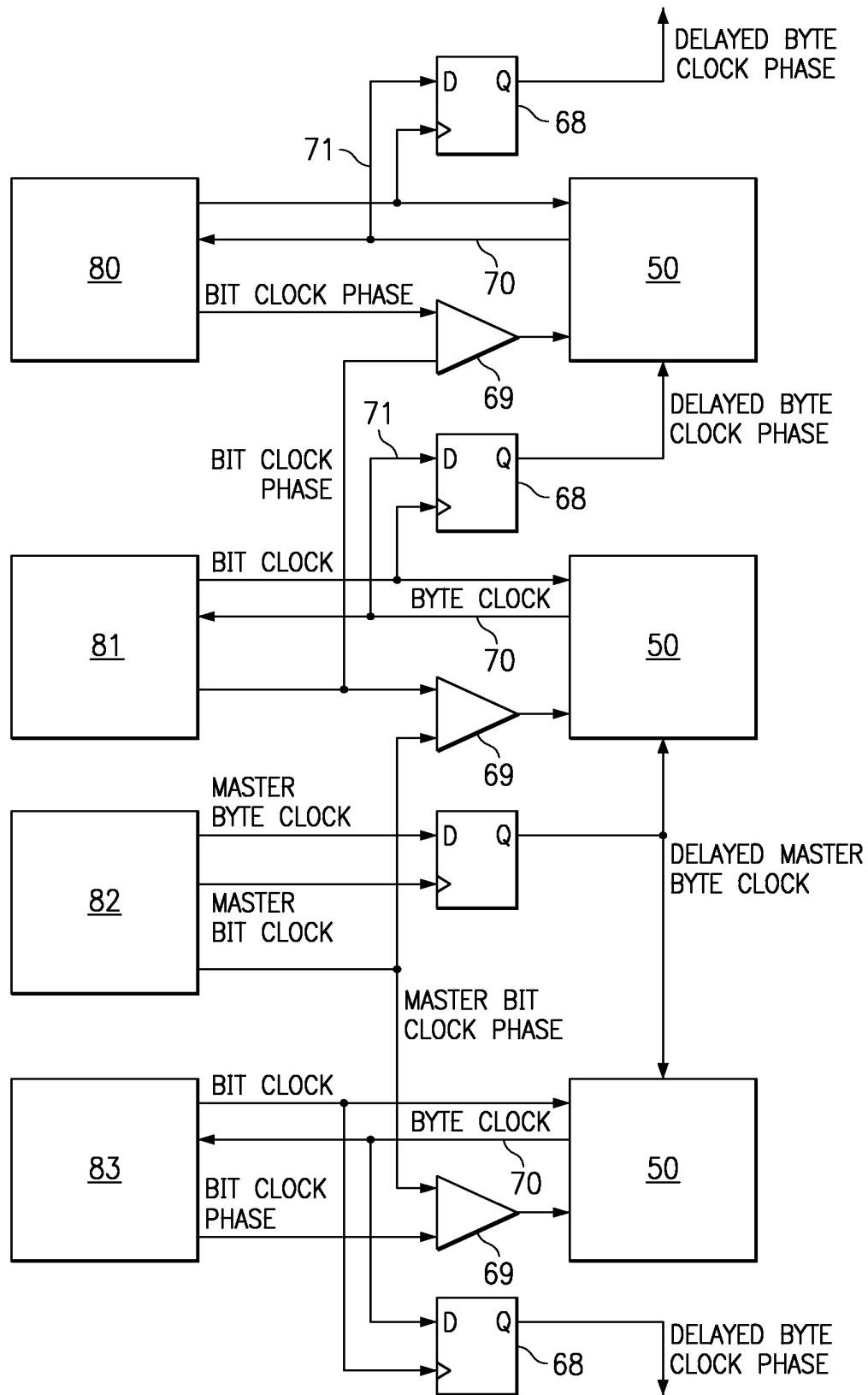
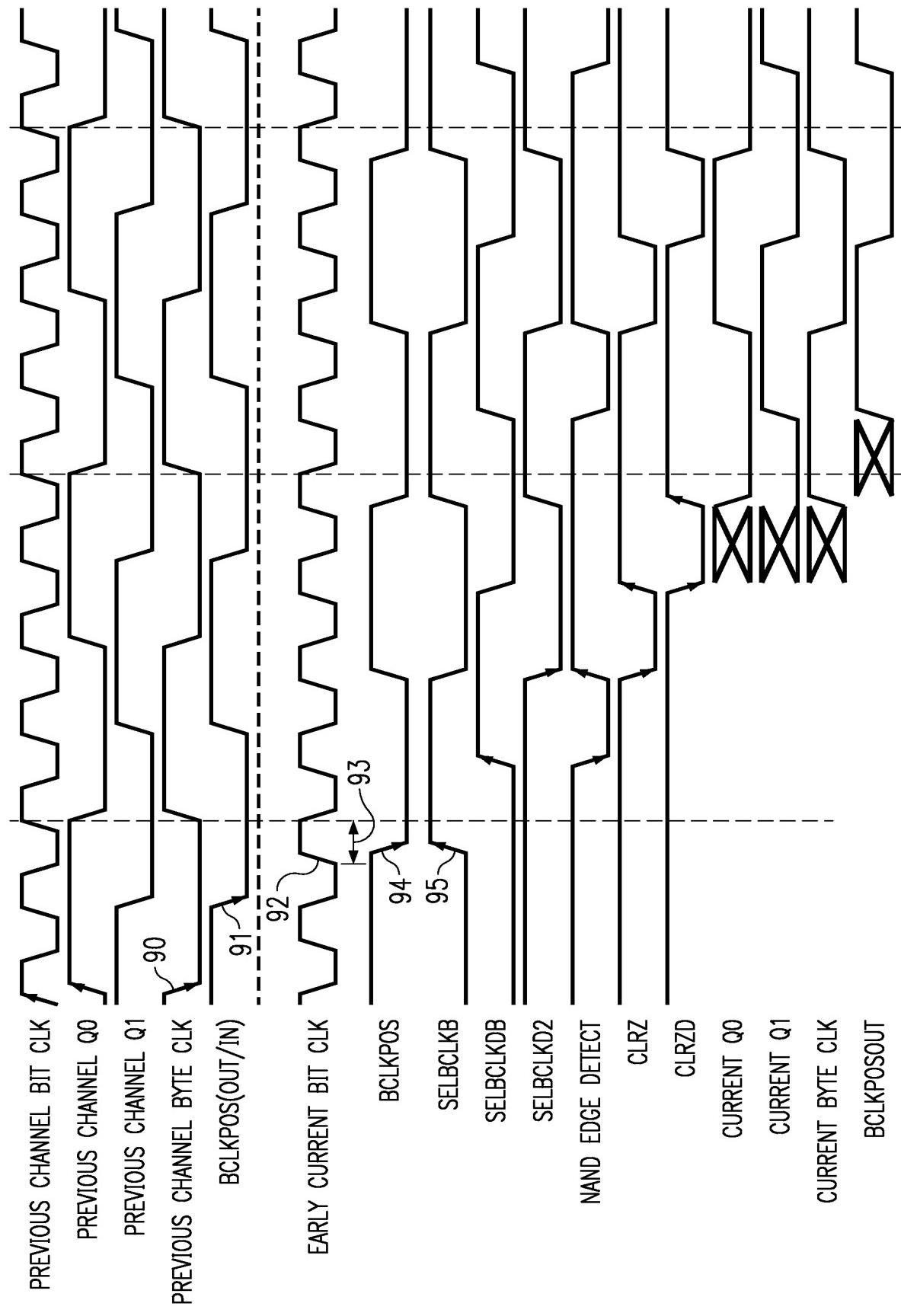


FIG. 18

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FIG. 19



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FIG. 20

